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Addressing technique employing both direct and **indirect register addressing**
HW Edwards Jr .. - US Patent 3,946,366, 1976 - Google Patents
... [54] **ADDRESSING** TECHNIQUE EMPLOYING BOTH DIRECT AND **INDIRECT REGISTER ADDRESSING**
[75] Inventor: Howard W. Edwards, Jr., Dracut, Mass. ...
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A Hasegawa, I Kawasaki, K Yamada, S Yoshioka, S ... - IEEE micro, 1995 - ieeexplore.ieee.org
... Addressing mode Instruction format Direct **register** **Indirect register** Postincrement
indirect register Predecrement **indirect register** Indirect register with ...
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... of modifying a microinstruction with operands specified by an instruction held in an alias **register**
A Carbine, FS Smith - US Patent 5,222,244, 1993 - Google Patents
... s9. g2 TABLE I **Indirect Indirect Register Addressing Address** Allowed in **Register**
Syntax **Address** these fields: source 1 src1 src1 sO srcl.src2.dst src 1 (high ...
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Memory bank and **register** allocation in software synthesis for ASIPs- ▶ ktupm.edu.sa [PDF]
A Sudarsanam, S Malik - 1995 IEEE/ACM International Conference on Computer-Aided ..., 1995 - ieeexplore.ieee.org
... When **register-indirect addressing** is used, the AGU generates the effective **address**. ...
Both memory accesses use **register-indirect addressing** - the ad- ...
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Instruction substitution mechanism in an instruction handling unit of a data processing system
DB Martin - US Patent 4,439,828, 1984 - Google Patents
... will be stored in the Opera- **indirect** substitute instruction ... tion **Register** 14, the
Instruction **Register** 24 will ... detector of the code and **address** generation phase ...
Cited by 33 - Related articles - Web Search - All 2 versions

A formal HDL and its use in the FM9001 verification
WA Hunt, C Brock - Philosophical Transactions: Physical Sciences and ..., 1992 - jstor.org
... **addressing** modes: **register** direct, **register indirect**, **register indirect** with
pre-increment, and **register indirect** with post-increment. ...
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Use of configuration registers to control access to multiple caches and nonvolatile stores
BC Beardsley, RR Knowlden, GA Spear - US Patent 5,640,530, 1997 - Google Patents
... of a storage path processor; degradation of system performance will occur should
this mG 5 js a block diagram showing the **indirect addressing** single point of ...
Cited by 19 - Related articles - Web Search - All 2 versions

Capability-based **addressing**- ▶ bgu.ac.il [PDF]
RS Fabry - 1974 - portal.acm.org
... and the main problem with the uniform **address** solution is ... segment for each process
and thus specifies **indirect** evaluation through a processor **register**. ...
Cited by 354 - Related articles - Web Search - All 6 versions

Signal processor memory management unit with **indirect addressing** using selectable offsets and modulo ...
BC Wang, ME Daly ... - US Patent 4,935,867, 1990 - Google Patents
... A-/B- DECODED **REGISTER** WRITE **ADDRESS** VALID 300o 301 A-/B- INTERNAL **ADDRESS** LATCH
VALID 302 B-INTERNAL **ADDRESS** BUFFER VALID 304 A-/B- **INDIRECT ADDRESS** UPDATE ...
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Method and system for **addressing** registers in a data processing unit in an **indirect addressing** mode
RC Agarwal, JJH Forrest, FG Gustavson, MA Johnson, ... - US Patent 5,890,222, 1999 - Google Patents
... It is yet another object of the present invention to provide an improved method
and system for **addressing register** files in an **indirect addressing** mode. ...
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Key authors: **S Malik** - **A Sudarsanam** - **Y Patt** - **G Araujo** - **W Hunt**

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